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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-00877 JW **DEFENDANTS' REPLY CLAIM CONSTRUCTION BRIEF FOR THE "TOP TEN" TERMS** Date: January 27, 2012 Judge: Hon. James Ware

HTC CORPORATION and HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-00882 JW
BARCO, N.V., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-05398 JW

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Cases

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'148 patent	U.S. Patent No. 6,598,148, issued July 22, 2003 (attached to the Otteson Decl. as Exhibit CC)
'336 patent	U.S. Patent No. 5,809,336, issued September 15, 1998 (attached to the Otteson Decl. as Exhibit DD)
'749 patent	U.S. Patent No. 5,440,749, issued August 8, 1995 (attached to the Otteson Decl. as Exhibit BB)
'890 patent	U.S. Patent No. 5,530,890, issued June 25, 1996 (attached to the Otteson Decl. as Exhibit AA)
Alliacense	Declaratory judgment defendant Alliacense Limited
Defendants or "TPL"	Declaratory judgment defendants Technology Properties Limited, Patriot Scientific Corporation and Alliacense Limited
JCCS	Joint Claims Construction Statement, filed November 23, 2011 (*Acer* Dkt. 307); Exhibits to the JCCS were filed as *Acer* Dkt. 305
Mar Decl.	Declaration of Eugene Mar in Support of Defendants' Opening Claim Construction Brief, filed December 9, 2010 (*Acer* Dkt. No. 213)
Otteson Decl.	Declaration of James C. Otteson in Support of Defendants' Reply Claim Construction Brief for the "Top Ten" Terms (filed December 23, 2011)
Otteson Reply Decl.	Declaration of James C. Otteson in Support of Defendants' Reply Claim Construction Brief for the "Top Ten" Terms (filed January 17, 2012)
Patriot	Defendant Patriot Scientific Corporation
Plaintiffs	Declaratory judgment plaintiffs Acer, Inc., Acer America Corporation, Barco, N.V., Gateway, Inc., HTC Corporation and HTC America, Inc.
TPL	Defendant Technology Properties Limited; "TPL" is also used throughout this brief to refer to all three declaratory judgment defendants

Introduction

Plaintiffs blithely refer to Mr. Moore as a "commercial failure" and characterize his inventions as "bizarre," suggesting that he is a patent-trolling crackpot. Nothing could be further from the truth. Over 90 industry leading electronics companies (such as Motorola, General Electric and Panasonic) have purchased licenses so that they can lawfully use the lessons of the patents-in-suit. These are not "nuisance value" licenses reached during litigation; these are significant royalty-bearing licenses recognizing the valuable contributions Mr. Moore made over the prior art. See *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998) (patentability shown by "licenses showing industry respect for the invention.")

Argument

I. CPU CLOCK-RELATED TERMS.

Plaintiffs' *Markman* brief ("Opp.") includes a general (and disputed) discussion of the clock-related terms (Opp. 1-3) before it addresses the five specific clock-related disputed terms. In this reply, Defendants will respond to the disputed terms in the order in which the specific terms are addressed by Plaintiffs.

A. Ring Oscillator.

Plaintiffs continue to argue that the term "ring oscillator" must be construed more narrowly than it was by Judge Ward in Texas because the patentee allegedly made a clear and unequivocal disavowal in the '148 patent reexamination to overcome the Talbot reference. Opp. at 3-6, 11-12. However, the PTO has repeatedly rejected ***the exact same argument***, finding that Talbot neither anticipates the '148 patent nor requires amendment of the claims.

The Talbot reference was one of the asserted bases for re-examination of both the '336 patent and the '148 patent. Otteson Reply Decl., Exs. EE, FF. Two separate examiners handling the reexaminations had before them (1) the Talbot reference, (2) the written advocacy of the re-examination requester, and, in the case of the '148 patent reexamination, (3) Judge Ward's construction of the term "ring oscillator" (the same construction Defendants propose here). Yet neither examiner required amendment of the claim term "ring oscillator," and neither found Talbot to anticipate.

Instead, in the '148 patent reexamination, the Examiner received the Patent Owner's written response filed February 26, 2008, explaining why Talbot was distinguishable. Otteson Decl. Ex. Y. Nothing in that written response could even arguably support the construction that Plaintiffs urge. After fully considering that response, the Examiner stated: "Patent Owner's arguments, filed 2/26/08 with respect to the rejections [based on Talbot] have been fully considered and are persuasive. Therefore, the rejection … has been withdrawn."[1] *Id.*, Ex. Z.

1. There was no "clear and unmistakable disavowal."

"Prosecution history ... cannot be used to limit the scope of a claim unless the **applicant** took a position before the PTO." *3M Innovative Props. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1373 (Fed. Cir. 2003) (emphasis added). The reason for requiring the disclaimer to come from the **applicant** rather than the **Examiner** is the recognition that sometimes the Examiner and applicant are talking past one another. *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1124 (Fed. Cir. 2004) (Where an "examiner and applicant [are] talking past one another" and "the record finally reflects the examiner's acquiescence to the claim language chosen by the applicant, [t]his is not clear evidence of the patentee's disavowal of claim scope.").

In the interview summary on which Plaintiffs rely, the Examiner summarized a face-to-face meeting among five individuals. Otteson Decl. Ex. X. The Examiner provided a three-sentence summary of the discussion of Talbot – clearly only shorthand for a full discussion that the patent owners agreed to submit in writing. He wrote: "The Examiner will reconsider the current rejection ***based on a forthcoming response***." *Id.* That longer discussion, submitted just eight days later, sets forth the several reasons Talbot is distinguishable. The Examiner expressly accepted that explanation, never mentioning his interview summary. Thus, the prosecution history as a whole demonstrates that there was no disclaimer. *Ecolab, Inc. v. FMC Corp.*, 569 F.3d 1335, 1342 (Fed. Cir. 2009) ("Even if an isolated statement appears to disclaim subject

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[1] Plaintiffs say that the Examiner's reliance on the written submission is just "TPL's speculation." Opp. 5:17. But the examiner wrote that he was persuaded by "Patent Owner's arguments, **filed 2/26/08**." Otteson Decl., Ex. Z (emphasis added). Thus, there is no speculation.

matter, the prosecution history as a whole may demonstrate that the patentee committed no clear and unmistakable disclaimers.")[2]

Allegedly disavowing statements must be both "so clear as to show reasonable clarity and deliberateness, and so unmistakable as to show unambiguous evidence of disclaimer" in order for a court to limit the meaning of a claim term. *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F3.d 1314, 1325 (Fed. Cir. 2003). Here, the alleged disavowing statement — "non-controllable" — is itself ambiguous, and would require further construction. That by itself establishes that there was no "clear and unambiguous" disclaimer. *Seachange Int'l, Inc. v. C-COR Inc.*, 413 F.3d 1361, 1373 (Fed. Cir. 2005) ("A disclaimer must be clear and unambiguous.") That ambiguity also confirms that Plaintiffs' proposed construction should be rejected, since the jury will have no way to determine what a "non-controllable" oscillator is. *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1378 (Fed. Cir. 2005) ("dust free" could not be interpreted to mean "very low dust" because the latter is a relative phrase and thus ambiguous and indefinite); *Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1256 (Fed. Cir. 2008) (rejecting patentee's proposed construction because "as used in the claims [the construction] is indefinite because it is ambiguous.").)

2. "in the environment" is unsupported and ambiguous.

Plaintiffs also seek to add an additional requirement to the construction of ring oscillator: "(2) variable based on the temperature, voltage, and process parameters **in the environment.**" The sole authority Plaintiffs recite for adding this limitation is a statement from an earlier Markman brief by Defendants. Opp. 4, fn.3 ("Part (2) of this construction is based on TPL's explanation of the term 'environment' in its previous claim construction briefing.") In fact, the cited portion of the "previously referenced claim construction briefing" was TPL's ***criticism*** of including "in the environment," because it is unsupported and ambiguous. See Doc. No. 221 in the Acer action

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[2] Nor was the patent owner obligated to correct the Examiner's mistake. "An applicant's silence in response to an examiner's characterization of a claim does not reflect the applicant's clear and unmistakable acquiescence to that characterization if the claim is eventually allowed on grounds unrelated to the examiner's unrebutted characterization." *3M Innovative Prop. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1373-74 (Fed. Cir. 2003); *Salazar v. Procter & Gamble Co.*, 414 F.3d 1342, 1346-47 (Fed. Cir. 2005) ("This court refuses to create a rule or presumption that the applicant in this case disavowed claim scope by silence.")

(02/11/2011 TPL Claim Construction Brief), at 17:16-19. The absurdity of relying on an opponent's brief criticizing your proposed claim construction as the sole support ***for*** the proposed construction is self-evident.

Moreover, as TPL's earlier brief explained, "in the environment" remains unsupported and ambiguous, and would necessitate its own construction. What "environment" should the jury look to? Temperature might be an environmental parameter, but are voltage and process environmental parameters? Plaintiffs' proposed construction introduces insoluble ambiguity into the claims; confirming that it is wrong. *Chimie v. PPG Indus., Inc.*, 402 F.3d at 1377 ("Courts construe claim terms in order to assign a fixed, unambiguous, legally operative meaning to the claim.")

3. The quoted portions of the patent and file history are not disclaimers.

Throughout Plaintiffs' brief, starting with the section on "ring oscillator" (Opp. 7-9), Plaintiffs quote statements from the specification and prosecution history describing the benefits of the invention over the prior art to argue that the patentee disclaimed anything in the prior art. This is a logical fallacy and misapplies the law on disclaimer.

Logically, it is fallacious to conclude that because a patentee touts that their invention includes A, B and C, while the prior art only has A and B, that the patentee is disclaiming A and B. Here, for example, the Plaintiffs include a series of quotes in which the patentee explains the benefits of the CPU clock on the same substrate as the CPU itself – *i.e.*, that variations due to the manufacturing process, voltage or temperature affect both the on-chip oscillator and the CPU in a similar manner, since both were created at the same time and reside on the same chip. '336 patent 17:2-10. The prior art systems lacked an on-chip oscillator that would vary at least by process, voltage and temperature. '336 Pros. Hist.; Mar Decl., Ex. E at TPL0001931 (Magar prior art uses "conventional crystal clock.")

Nothing in these quotations suggests that the on-chip clock must be "uncontrollable" simply because the prior art off-chip clocks were controllable. The described improvement is in having an on-chip oscillator for the CPU as opposed to an off-chip oscillator for the CPU— not an oscillator that is "non-controllable" versus one that is "controllable." Legally, the fact that the

patentee describes a benefit of an invention in the specification or prosecution history does not mean that every claim must be construed to require that benefit. *See Phillips v. AWH Corp*., 415 F.3d 1303, 1327 (Fed. Cir. 2005) ("We have held that '[t]he fact that a patent asserts that an invention achieves several objectives does not require that each of the claims be construed as limited to structures that are capable of achieving all of the objectives."); *Northrop Grumman Corp. v. Intel Corp*., 325 F.3d 1346, 1355 (Fed. Cir. 2003) (rejecting narrow construction limited to ensure presence of certain advantages). These logical and legal fallacies wholly discredit Plaintiffs' arguments.

4. The terms "ring oscillator," "entire oscillator" and "variable speed clock" are different.

Plaintiffs argue that the terms "ring oscillator," "entire oscillator" and "variable speed clock" are the same and should be construed identically. They are not the same. The terms "entire oscillator" ('336 patent Claim 6) and "variable speed clock" ('336 Claim 10) cannot be construed to mean "ring oscillator" without vitiating dependent claims 9 and 15 of the '336 patent.[3] See *Nazomi Commc'ns, Inc. v. Arm Holdings, PLC*, 403 F.3d 1364, 1370 (Fed. Cir. 2005) ("[C]laim differentiation 'normally means that limitations stated in dependent claims are not to be read into the independent claim from which they depend.'"); *Trintec Industrial, Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 1296 (Fed. Cir. 2002) (holding that where claim terms are worded differently, each "imparts a different scope to the claim in which it appears.")

Plaintiffs ask the Court to treat these terms identically, but the "examiner disclaimer" argument that Plaintiffs make (and Defendants dispute) only relates to the term "ring oscillator." The Examiner interview occurred during the reexamination of the '148 patent. Only claims 4 and 8 of the '148 patent were the subject of the interview, and those claims were drawn to "ring oscillator," and not "variable speed clock" or "entire oscillator." See Interview Summary, Otteson Decl. Ex. X ("Claim(s) discussed: 4 and 8.") Thus, even if the Court were to somehow accept the

[3] Dependent claim 9 reads: "[t]he microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator." Dependent claim 15 reads "[t]he microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator."

Plaintiffs' disclaimer argument, it only would apply to term "ring oscillator" and not "variable speed clock" or "entire oscillator."

B. Providing an Entire Variable Speed Clock Disposed upon Said Integrated Circuit Substrate.

The next dispute is over Plaintiffs' attempt to re-construe Judge Ward's prior construction of "an entire ring oscillator variable speed system clock in a single integrated circuit" to exclude the words "directly" and "command input." Plaintiffs' begin by spending considerable time discussing the prosecution history relating to the references Magar and Sheets. Opp. 7-9. Magar and Sheets were references that lacked the on-chip oscillator (of the '336 and accused devices), and which therefore relied directly on an external clock signal to generate the CPU clock. *See* '336 Pros. Hist.; [Acer Dkt. 213-214] Mar Decl., Ex. C at TPL0001905 (invention "contemplates providing a ring oscillator clock and microprocessor within the same integrated circuit" rather than prior art's "provision of frequency control information to an external clock."); '336 Pros. Hist.; Mar Decl., Ex. D at TPL0001920 (arguing "[i]n Sheets [], a command input is required to change the clock speed."); '336 Pros. Hist.; Mar Decl., Ex. E at TPL0001931 (Magar prior art uses a "conventional crystal clock.")

Like the Plaintiffs here, the Texas defendants argued that by distinguishing Magar and Sheets, TPL disclaimed any use of an off-chip signal whatsoever. Judge Ward, however, rejected that argument. Before Judge Ward, TPL argued that, properly understood in context, this was at most a disclaimer of ***direct use*** of the off-chip clock ***to generate*** the CPU clock in systems that have no on-chip oscillator of their own, such as those of Sheets and Magar. Ward at 11-12 ("[T]he defendants argue that the applicant disclaimed ***use*** of a control signal and an external crystal/clock generator in order to distinguish over prior art. … the [patentees] argue that, although an external crystal is not ***directly used to generate*** a system clock signal, the external crystal can be ***used*** as a reference signal to account for delay across certain circuit elements.") (emphasis added). Judge Ward agreed, and construed the term to exclude only ***direct reliance*** on an off-chip signal to generate the CPU clock—not ***any*** use of an off-chip signal.

Plaintiffs urge that by the patentee distinguishing Talbot in reexamination, the claims cannot cover any features found in Talbot. Opp. 12. Plaintiffs' argument is contrary to law. The Supreme Court, in *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418-19 (2007), explained that "inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." Thus, the fact that the claimed invention *as a whole* was an advance over Talbot does not mean that every aspect of Talbot was disclaimed. Nothing in the reexamination proceedings subsequent to Judge Ward's construction supports narrowing the claim to require ***no*** use (direct or otherwise) of the off-chip clock signal.

C. Clocking Said CPU.

Plaintiffs are once again seeking to narrow a construction from Judge Ward, even though the Texas Court already considered—and rejected—the exact same argument. *See* Ward 13-15 (Mar Decl., Ex. A) (rejecting Texas defendants' arguments relying on the same specification cites ['336 patent 17:1-2, Mar Decl., Ex. B] and prosecution history [Mar Decl., Ex. C, TPL0001905-06] that Plaintiffs rely on here to argue that the CPU's processing frequency must operate at the "fastest safe operating speed"). Plaintiffs wrongly suggest that their construction is required because the patent only discloses a single embodiment. The specification of the patents-in-suit discloses multiple embodiments of the various inventions; so many that the PTO required the applicants to divide the original application into 10 separate applications. Otteson Reply Decl., Ex. GG. Indeed, Plaintiffs' brief refers to various embodiments. Opp. 19 ("the specification describes a different and unclaimed embodiment") ("Figure 9 shows 'a layout diagram of a second embodiment of a microprocessor.'"), Opp. 25 (arguing that Figure 21 is a different embodiment).

Even in cases where a single embodiment is disclosed, importation of the specification into the claims is improper. *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004) ("[E]ven where a patent describes only a single embodiment, claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction.")

Plaintiffs' proposed construction—"it will always execute at the maximum frequency possible, but never too fast"—is impermissibly vague and ambiguous, providing no guidance whatsoever on how to determine infringement or validity. There is no criteria specified that would enable the jury to determine the "maximum frequency possible" or whether the CPU is going "too fast." Plaintiffs' proposed construction thus hinders, rather than helps, the trier of fact and must be rejected. *Chimie v. PPG Industries, Inc.*, 402 F.3d at 1378 (rejecting proposed construction calling for "very low dust" as ambiguous and indefinite).

Further, Plaintiffs distort the prosecution history to suggest that the applicants distinguished Sheets by relying upon the "aspect" of the invention that the "CPU executes at the fastest speed possible." Opp. 14. In fact, the applicants distinguished Sheets because it did not have an ***on-chip*** oscillator; and specifically required a "command input control signal" to vary the frequency. '336 Pros. Hist., Mar Decl., Ex. C, TPL0001904 ("the present invention is directed to a system and method for clocking a central processing unit disposed within the same integrated circuit…"). The patentee then amended the relevant claims to "explicitly recite that the ring oscillator and microprocessor are provided within the same integrated circuit." *Id.* Thus, the basis for distinguishing Sheets was the presence of an on-chip oscillator, not the frequency of the CPU. Judge Ward's construction was correct and should be adopted here.

D. <u>Operates Asynchronously To</u>.

Construing "operates asynchronously" is straightforward because, as explained in Defendants' opening brief (Brief 12-13), the patentee acted as his own lexicographer by providing a textbook definition of "asynchronous" during prosecution.[4] *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) ("A claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history."). Plaintiffs' argument (Opp. 15) that offering a definition in prosecution must be ignored as "self-serving" would vitiate the *CCS*

[4] Plaintiffs' suggestion that the Court consider other portions of this book, even though they are not part of the intrinsic record (Opp. 16, Chen Decl., Ex. 10), should be rejected. *Phillips*, 415 F.3d at 1317 (cautioning against reliance on extrinsic evidence).

Fitness/lexicography doctrine entirely, since ***everything*** done by the patentee during prosecution would be considered "self-serving" under Plaintiffs' theory. [5]

> Moreover, Defendants' definition is consistent with the specification:
>
> The central processing unit and the ring counter variable speed system clock are provided in a single integrated circuit. An input/output interface is connected to exchange coupling control signals, addresses and data with the input/output interface. ***A second clock independent of the ring counter variable speed system clock*** is connected to the input/output interface. ['336 patent; 3:26:35 (emphasis added).]

It is also consistent with the claims:

> Claim 11: ". . . a second clock ***independent*** of said ring oscillator variable speed system clock . . ."
>
> Claim 13: ". . . an off-chip external clock, ***independent*** of said oscillator. . ."
>
> Claim 16: ". . . said off-chip external clock is operative at a frequency ***independent*** of a clock frequency of said variable speed clock . . ."

Thus, Defendants' construction is both supported by the prosecution history, and the consistent usage of these terms in both the specification and the claims, and should be adopted. *Edwards Lifesciences v. Cook Inc.*, 582 F.3d 1322, 1329 (Fed. Cir. 2009) ("The interchangeable use of the two terms is akin to a definition equating the two.")

E. As a Function of Parameter Variation.

The term "as a function of parameter variation" is so straightforward that the Court will likely find it requires no construction at all. If construed, however, Defendants' proposed construction is correct because the intrinsic evidence contemplates that clock rate and processing frequency can vary based on a variety of factors. Defendants' construction conveys the notion with which the inventors were concerned: by placing the on-chip oscillator on the same silicon die as the CPU, the clock and the CPU would be similarly affected by these factors. The specification provides a clear example of what is meant:

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[5] Plaintiffs improperly rely on an irrelevant statement made during prosecution regarding then-pending dependent claim 8 that was eventually canceled. Opp. 15: 7-11. Because the statement was made only with respect to a specific limitation ("synchronous") of a now-canceled claim, it cannot operate as a disclaimer for a claim that does not include that limitation. *Go-Light, Inc. v. Wal-Mart Stores, Inc.*, 355 F.3d 1327, 1332 (Fed. Cir. 2004).

> For example, if the processing of a particular die is not good resulting in ***slow transistors***, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates, it too will ***operate slower*** (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly. ['336 patent 17:2-10 (emphasis added).]

Plaintiffs offer an unfounded construction that requires that the effect of the parameter variation be "determined" in a strict mathematical sense. Plaintiffs urge that, "for a given combination of temperature, voltage and process parameters, the CPU's and the on-chip oscillator's frequencies should be reproducible." Opp. 16. As the sole support for this alleged requirement, Plaintiffs cite a passage from the specification that says "[a]t room temperature, the frequency will be **in the neighborhood of** 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ." '336 patent at 16:60-63 (emphasis added). The phrase "in the neighborhood of" is the ***exact opposite*** of the mathematical precision that Plaintiffs suggest these words require, as is the use of the terms "slow" and "operate slower" in the example excerpted above.

Nothing in the specification requires a predetermined mathematical formula for assessing the impact of temperature, voltage or process parameters; indeed there is no teaching of how that would be determined. Plaintiffs' proposed construction must be rejected.

II. MICROPROCESSOR ARCHITECTURE RELATED TERMS.

A. Separate Direct Memory Access Central Processing Unit.

Plaintiffs read two extraneous limitations into the claim term "separate DMA CPU," ***requiring*** it to (1) "fetch and execute instructions," and (2) function "without using the main central processing unit." As support, Plaintiffs cite two statements from the specification describing beneficial aspects of an embodiment. Plaintiffs' construction flatly violates the rule against reading embodiments and objectives into the claims. *Phillips*, 415 F.3d at 1327.

First, Plaintiffs ask the Court to require that the DMA CPU "*fetches and executes instructions.*" Plaintiffs cite to the description of the embodiment in Figure 2, wherein "[t]he DMA CPU 72 controls itself and ***has the ability to*** fetch and execute instructions." Opp. 18:10-12 (emphasis added). Of course, a statement in the specification that an embodiment "has the ability" to do something is not a basis to import that as a requirement of the claims. Moreover, Plaintiffs'

construction requires the Court to ignore the alternate embodiment shown in Figure 9 as "unclaimed subject matter" because it supports Defendants' construction and refutes the Plaintiffs' construction. Opp. 18:20–19:26 (characterizing Figure 9 as an "unclaimed embodiment.") Plaintiffs' arguments are unavailing.

Next, Plaintiffs seek to require the DMA CPU to function "*without using the main central processing unit*." Plaintiffs quote the "Summary of the Invention" of the '890 patent, wherein it explains that "[i]t is a further object of the invention to provide a high performance microprocessor in which DMA ***does not require*** use of the main CPU during DMA requests and responses'" Opp. 18:14-17 (citing '890 patent at 2:1-5) (emphasis added). Plaintiffs' argument ignores the rule that an object of the invention should not be read into the claims.[6] Moreover, the words "does not require" does not mandate that the DMA CPU ***cannot use*** the main CPU. Moreover, Plaintiffs' expert, Dr. Wolfe, testified that the main CPU can interact with the DMA CPU to at least initiate memory transfer – and even Plaintiffs themselves concede this point. Opp. 19:27-20:6.[7]

Further, the microprocessor 310 in Figure 9 is described as "equivalent to the microprocessor 50 in FIGS. 1-8." *Id.*, 9:5-6. In describing specific differences between the embodiments illustrated in Figures 2 and 9, the inventors note that "the DMA processor 72 of the microprocessor 50 has been replaced with a more traditional DMA controller 314." *Id.*, 12:63-65. The inventors then go on to describe that that the DMA (indicated as DMA CPU 314 in Figure 9) performs, *inter alia*, 8-bit parallel I/O. *Id.*, 13:2, *see also* 11:45-50. In other words, the DMA CPU 314 illustrated in Figure 9 is structurally similar and accomplishes the same function as does the DMA CPU 72 illustrated in Figures 2, 4 and 5: it is part of an electronic circuit for reading and writing memory. Plaintiffs' proposed construction is improper as it would exclude this

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[6] *E-Pass Techs., Inc. v. 3Com Corp.*, 343 F.3d 1364, 1370 (Fed. Cir. 2003) ("An invention may possess a number of advantages or purposes, and there is no requirement that every claim directed to that invention ... encompass all of them.")

[7] Plaintiffs suggest that Dr. Wolfe only admitted to "initiating" direct memory access and not "performing" direct memory access. Plaintiffs do not explain how a jury would determine the difference, or why both would not be prohibited under Plaintiffs' flawed construction.

preferred embodiment. For the foregoing reasons, TPL's proposed construction should be adopted.

B. Push Down Stack Connected to Said ALU.

A push down stack has a well-known meaning to those skilled in the art, and the parties seem to be in agreement on the fact that it means a last-in, first-out ("LIFO") data storage structure, wherein the last item placed (or pushed) onto the stack is the first item removed (or popped) from the stack. Opp. 20:8-14. The disagreement arises from the Plaintiffs' inclusion of extraneous limitations taken from embodiments or statements made by an Examiner during prosecution. For example, Plaintiffs propose that "push down stack" have a "top" and a "bottom" and a direction of "propagation" from top to bottom. These limitations would read out stacks that, for example, have a bottom-to-top, circular or virtual orientation. Since this is a microprocessor patent, the Plaintiffs' attempt to impart a physical orientation makes no sense, and will only confuse the jury."

The claim further provides for a push down stack "connected to" said ALU. Plaintiffs propose that this covers only stacks having a "top item register" and a "next item register" that are both "**directly coupled to**" the ALU "such that source and destination address are not used." Plaintiffs are essentially arguing that this claim term is limited to the exact configuration shown in Figure 2. This attempt to restrict the claims to a specific figure is unwarranted for numerous reasons.

1. The Examiner's characterization that inputted items in a stack propagate from one end to another is inapplicable.

Plaintiffs argue the Court should import into the claim construction the phrase "wherein any previously stored items propagate towards the bottom by one data storage element when a new item is stored in the top data storage element" because ***the Examiner*** characterized a push down stack "such that inputted items propagate from one end of the stack to another via the stages

in the stack."[8] Opp. 21:1-8. Plaintiffs are incorrect. "Prosecution history ... cannot be used to limit the scope of a claim unless ***the applicant*** took a position before the PTO." *3M Innovative Props.*, 350 F.3d at 1373 (emphasis added). Here, applicant responded by stating that the claimed stack structure was conventional (e.g., uses stack pointers) and that top and next were "in addition to the conventional construction of the first push down stack." '749 Office Action response July 6, 1993 at 9. Thus, when read in full, the prosecution history Plaintiffs rely on actually supports Defendants' construction, and not the Plaintiffs'.

2. The "connection" between the push down stack and the ALU is not limited to "direct coupling … such that source and destination addresses are not used."

Although the claim expressly specifies the push down stack need only be "***connected to***" the ALU, Plaintiffs argue that the Court should limit the invention to embodiments where the push down stack is "***directly coupled to***" the ALU. In other words, no intervening circuit elements could exist between the push down stack and the ALU.

The patentees clearly appreciated the difference between the broader term "connected to" and the narrower term "directly coupled to"—and claimed the broader term. The specification of the '749 patent uses the term "connected to," "***directly*** connected to" (1:61-62) and "***directly*** coupled to" (19:7) (emphasis added).

For example, the specification uses the term "connected to" to characterize the embodiment shown in Figure 21 as follows: "In yet another aspect of the invention, a push down stack is ***connected to*** the arithmetic logic unit." '749 patent, 3:36-37 (emphasis added). The specification goes on to describe this embodiment as including up to three stack segments and three stack pointers. '749 patent, 3:50-55 ("a ***first pointer*** is connected to the ***first plurality of stack elements***, a ***second pointer*** is connected to the ***second plurality of stack elements*** and a ***third pointer*** is connected to the ***third plurality of stack elements***.") (emphasis added). Since

[8] See Chen Decl., Ex. 14, wherein the Examiner wrote: "With respect to claim 6, the components (means for storing a top item, means for storing a next item and the at least one stack register) of the first push down stack, as recited do not appear to render the push down stack to operate as a stack. Note that a stack is such that inputted items propagate from one end of the stack to another via the stages in the stack. The stack as recited in the claim does not do that."

Figures 2 and 13 only contain a single first push down stack segment and a single stack pointer, this discussion is clearly directed at Figure 21, the only figure containing three stack segments and three pointers.[9] So while Plaintiffs argue that Figure 21 is not covered by this limitation because it does not show direct coupling, the patentee's use of the words "connected to" to describe the embodiment shown in Figure 21 means that "connected to" does not require direct coupling between the stack and the ALU. *See e.g., Mass Engineered Design, Inc. v. Ergotron, Inc.*, 559 F.Supp.2d 740, 752 (E.D. Tex. 2008) ("The term 'connected to' has its plain and ordinary meaning … which is simply a 'connection.'"); *Animatics Corp. v. Quicksilver Controls, Inc.*, 102 Fed. Appx. 659, 667-68 (Fed. Cir. 2004) (Reversing as too narrow district court claim construction that term "connected to" required an electrical connection rather than a logical connection).

In a somewhat convoluted argument, Plaintiffs argue that "direct coupling … such that source and destination addresses are not used" is "an essential aspect of the claimed invention." Opp. 22:6-24:1. However, stack pointers comprise source and destination addresses and stack pointers are used in at least two alternate embodiments beyond that disclosed in Figure 2. Thus, Defendants respectfully ask the Court to reject Plaintiffs' attempt to limit the claim term to a particular embodiment, that of Figure 2.

3. Plaintiffs' means-plus-function argument is unavailing.

Plaintiffs also argue that the means-plus-function elements following the claim term under construction supports their "directly coupled to" construction. Plaintiffs are again mistaken. First, the means-plus-function limitations are directed to "means for storing" and **not** "connected to." Second, Plaintiffs disregard the structure disclosed in Figure 21, which show the use of stack pointers in conjunction with a first push down stack. *See* '749 patent, 3:36-66. Since both Figure 13 and Figure 21 disclose a "means for storing," they are necessarily available for use with the claim under 35 U.S.C. §112, ¶6, which mandates that such claims "shall be construed to cover the

[9] This alternative embodiment expressly contemplates the use of stack pointers, which by definition contain an ***address*** pointing to a stack. '749 patent, 11:6.

corresponding structure, material, or acts described in the specification and equivalents thereof." *Micro Chem., Inc. v. Great Plains Chem. Co., Inc.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999) ("When multiple embodiments in the specification correspond to the claimed function, proper application of § 112 ¶ 6 generally reads the claim element to embrace each of those embodiments.") For all the foregoing reasons, TPL's proposed construction should be adopted.

C. Supply the Multiple Sequential Instructions to Said Central Processing Unit Integrated Circuit During a Single Memory Cycle.

Plaintiffs and Defendants agree on much of the construction for the limitation: "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle." Both sides agree the phrase should be construed to mean, at least:

> provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle.

That construction is sufficient, and should be adopted.

Plaintiffs argue, however, the Court should limit the meaning of the claim language further by tacking on the following phrase: "*without using a prefetch buffer or a one- instruction-wide instruction buffer, that supplies one instruction at a time*." Plaintiffs' purported support for their position provides no support at all.

Plaintiffs rely on four statements made by the patentee during re-examination of the '749 patent. Opp. 27:1-28-5. None of these statements is a clear disavowal of either a *prefetch buffer* ***or*** a *one-instruction-wide instruction buffer*. The only statement that even mentions "prefetch buffer" makes clear that TPL was distinguishing the supplying of instructions to the CPU one at a time – not the use of a prefetch buffer. In distinguishing the Edwards reference, TPL argued "[f]etching multiple instructions into a prefetch buffer ***and then supplying them one at a time is not sufficient to meet the claim limitation*** – the supplying of 'multiple sequential instructions to a CPU during a single memory cycle.'"[10] Nothing in this statement restricts the use of a prefetch

[10] Amendment, 1/19/10 at 26 of 58 (Chen Decl., Ex. 16 (emphasis added).

buffer generally, as long as the device "provide[s] multiple sequential instructions in parallel to said central processing unit *in a single memory cycle*."

The remaining three statements from the '749 patent reexamination cited by Plaintiffs similarly fail to support the restrictions Plaintiffs seek to impose. None of these statements mentions a "prefetch buffer" ***or*** a "one-instruction-wide buffer." Moreover, each statement expressly distinguishes the prior art reference on the same basis: (a) "the instructions are supplied to the CPU one at a time,"[11] (b) "although two instructions might be fetched at the same time, one instruction is supplied to the CPU at a time,"[12] and (c) "the 'during a single memory cycle' limitation is not satisfied by supplying only one instruction to the CPU at a time."[13]

Thus, there are no clear and unmistakable disavowals of a prefetch buffer or a one-instruction-wide buffer, and the remaining portion of the construction is agreed upon and should be adopted.

D. Instruction Register.

Plaintiffs and Defendants agree on much of the construction for the limitation: "instruction register." Both sides agree the phrase should be construed to mean, at least:

> register that receives and holds one or more instructions for supplying to circuits that interpret instructions

This construction is sufficient and should be adopted. Indeed, the construction provides a precise and accurate definition of an "instruction register."

Plaintiffs argue that the Court should tack on the following phrase: "*in which any operand that is present must be right-justified in the register*." Plaintiffs lack support for this additional limitation.

1. The claim limitation refers to an "instruction register," not "operands" or "instruction groups."

Plaintiffs' entire argument sidesteps the clear meaning of the term "instruction register," and instead focuses on a distracting and irrelevant discussion of "operands" and "opcodes" and the

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[11] Amendment 1/19/10 at 45 of 58 (Chen Decl., Ex. 16).
[12] 11/29/2010 Interview Summary at 19-20 of 35 (Chen Decl., Ex. 18).
[13] 11/29/2010 Remarks at 13 of 35 (Chen Decl. 18).

manner in which operands might appear in an "instruction group." Further, the term "instruction group" and the positioning of operands within an instruction group was only at issue in the '584 patent, which is not at issue in the current litigation. TPL urges the Court to reject Plaintiffs' attempt to ignore the clear meaning of "instruction register."

2. Judge Ward's construction of "instruction group" is inapplicable to the construction of the term "instruction register."

Plaintiffs argue that Judge Ward's construction of the term "instruction ***group***," in U.S. Pat. No. 5,784,584 (the '584 patent), necessarily controls the meaning of "instruction ***register***," in the '749 patent. Plaintiffs' argument overlooks and mischaracterizes several key aspects of Judge Ward's prior ruling, and should be rejected.

a. Significant differences in the claimed subject matter of the '749 and '584 patents require separate constructions.

The '584 patent resulted from a divisional application from the '749 patent; thus the '584 patent carved out separate subject matter from the '749 parent. The '584's "instruction groups" describe how instructions and data are organized in memory, whereas the "instruction registers" of the '749 patent refer to a structural component that can supply multiple sequential instructions to a CPU during a single memory cycle. In other words, "instruction groups" refer to data (1's and 0's), while an "instruction register" refers to a physical element. Plaintiffs' attempt to ignore these significant distinctions between the claim terms of two different patents ignores controlling authority. Where "related patents are similar, [but] their claims are not identical," courts must independently construe the claims in each patent. *ResQNet.com, Inc. v. Lansa, Inc.*, 346 F.3d 1374, 1382 (Fed. Cir. 2003). Plaintiffs' argument that Judge Ward's construction of "instruction group" controls the construction of "instruction register" is simply incorrect.

b. Judge Ward's construction of the term "instruction group" from the '584 patent) to include right-justification of *data* may have been consistent with the '584 claim language—but is not the structural "instruction register" of the '749 patent.

Judge Ward construed original claim 29 of the '584 patent, which reads:

> In a microprocessor system including a central processing unit, memory, and an instruction register, a method for providing instructions and operands from said memory to said [CPU] comprising the steps of providing ***instruction groups*** to said instruction register from said memory wherein certain of said ***instruction groups*** include at least one instruction that, when executed, causes an access to an operand or an instruction or both, said operand or instruction being located at a predetermined position from a boundary of said ***instruction groups*** ….

The ***instruction groups*** recited in claim 29 contained an "operand or instruction being located at a predetermined position from a boundary" of the claimed instruction groups. The ability to locate instructions – again, ***data*** (1's and 0's) – by having them at a predetermined location was critical to the operation of the '584 system. Thus, Judge Ward's construction of "instruction groups" to include right-justified operands is consistent with the claim language of the '584 patent.

The relevant term in claim 1 of the '749 patent, on the other hand, involves a structural hardware component – not a command or data:

> A microprocessor system … wherein the microprocessor system comprises an ***instruction register*** configured to store the multiple sequential instructions and from which the multiple sequential instructions are accessed and decoded ….

'749 patent (Re-exam), 1:29, 1:57-60. Unlike the '584 patent claims, there is no requirement for how ***data*** (*e.g.*, multiple sequential instructions) are arranged within the '749 patent's physical "instruction register." For example, nothing in '749 claim 1 requires that "operands" in the data must be "right justified" in the register. Indeed, claim 1 only requires that the instruction register be configured to hold two or more sequential instructions from which the instructions are accessed and decoded. This is consistent with TPL's proposed construction, but not Plaintiffs'.

E. Multiple Sequential Instructions.

The parties largely agree on the construction of "multiple sequential instructions": "two or more instructions in sequence (or in a program sequence)." This construction is sufficient, and should be adopted. But again, Plaintiffs argue that the Court should tack on another unnecessary limitation: "*in which any operand that is present must be right-justified in the register*." Nothing in the intrinsic evidence requires this limitation.

Plaintiffs incorrectly argue that "multiple sequential instructions" is synonymous with "instruction group." Opp. 30:15-22. Although "*multiple* sequential instructions" must obviously

include at least two or more instructions in sequence (as the parties agree), an "instruction group" does not satisfy this requirement. As the '584 patent points out: "An instruction group may contain from ***one*** to four instructions." '584 patent, 19:18-19 (emphasis added). Thus, an instruction group with a single instruction is ***not*** synonymous with "multiple sequential instructions," which require two or more instructions.

Conclusion

For the foregoing reasons, Defendants respectfully ask the Court to enter an order adopting TPL's proposed claims constructions.

Dated: January 17, 2012

Respectfully submitted,

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